111 and **113** and the transparent electrode **115**. The source/drain portions **117** can be formed via a deposition process, such as a thin film deposition process, and particularly using chemical vapor deposition (CVD), physical vapor deposition (PVD), atomic layer deposition (ALD), ion implantation, or any combination thereof.

[0052] The source/drain portions **117** generally includes a conductive material conventionally used in forming source/drain portions of semiconductor devices, such as a heavily doped semiconductor material or a metal-containing material, such as a metal oxide, a metal nitride, a metal-semiconductor material, a metal alloy, or any combination thereof. Particular dopant materials can include boron, arsenic, and phosphorous. According to one embodiment, the source/drain portions **117** include a metal such as aluminum, chromium, tantalum, tungsten, or alloys thereof. Typically, the source/drain portions **117** have an average thickness of not greater than about 500 nm, and particularly within a range between about 100 nm to about 300 nm.

[0053] Referring to FIG. **1**H, after forming the source/drain portions **117** in FIG. **1**G, formation of the bottom gate transistor can include formation of a passivation layer **119**. According to one embodiment, the passivation layer **119** overlies the transistor structure (i.e., gate electrode **105**, semiconducting layers **111** and **113**, and source/drain portions **117**) and a portion of the transparent electrode **115**. The passivation layer **119** can be formed via a deposition process, such as a thin film deposition process, and particularly using chemical vapor deposition (CVD), physical vapor deposition (PVD) (e.g., sputtering) or combinations thereof.

[0054] The passivation layer **119** generally includes an insulating material. Particularly suitable insulating materials can include nitrides and oxides or combinations thereof. In one embodiment, the insulating layer includes a nitride, and particularly includes silicon nitride (SiN_x). In another embodiment, the passivation layer **119** includes a combination of an oxide and nitride, and particularly can include SiO_xN_y. Typically, the average thickness of the passivation layer **119** is not greater than about 500 nm, and particularly within a range between about 100 nm to about 300 nm.

[0055] In addition to the substrate having the TFT array and pixels, a fully assembled LCD can include a separate substrate, particularly a color filter substrate. The color filter substrate includes a series of red, green, and blue sub-pixels on a glass substrate that is separate from the substrate containing the TFT array and pixels. Generally, the color filters can be made with either dyes or pigments. Formation of the color filters includes forming unit dots; each unit dot having a red, green, and blue sub-pixel to allow each unit dot the ability to form a spectrum of colors. Formation of the color filters can include utilizing coloring methods such as dyeing, diffusion, electro-deposition, and printing. Moreover, formation of the color filters on the color filter substrate can include formation of color resists, particularly one for each color, which are formed by patterned masks which can later be exposed and developed, using UV radiation, to define red, green, and blue sub-pixels. Additionally, a black resin can be used to fill voids between the sub-pixels to limit reflectivity and improve the color generated by the LCD.

[0056] Generally, after forming the unit dots, a protective film can be formed over the color filter layer. Such a protective film can include an oxide or nitride. Moreover, after the formation of the protective film, a transparent electrode can be formed using the same techniques and materials as was used to form the transparent electrode on the substrate containing the array of TFTs and pixels.

[0057] After formation of the TFT array substrate and the color filter substrate, the substrates can be scored and sectioned to appropriate sizes to form individual LCD panels. Each panel will include a TFT array panel and a color filter panel thus forming a LCD device. The panels can be joined together within a sealant such that the pixel regions on the TFT substrate and the color filter regions on the color filter substrate are aligned.

[0058] Referring to FIG. **2**, a cross-sectional diagram of a portion of a LCD **200** is illustrated. The LCD **200** includes a TFT-array panel **201**, including a TFT **205**, a pixel electrode **206**, a polarizer **209**, and an alignment layer **207** overlying the TFT **205** and pixel electrodes **206**. The TFT-array panel **201** can further include a bonding pad. The LCD **200** further includes a color filter panel **203** which includes a color filter **211** and a black matrix layer **213** underlying the color filter **211**. The color filter panel **203** further includes a polarizer **217** overlying the color filter panels **203** and a transparent electrode **214** underlying the black filter. An alignment layer **215** underlies the transparent electrode **214**, black matrix layer **213** and the color filter **211**. The alignment layers **207** and **215** aid the alignment of the liquid crystals **217** between the panels **201** and **203** which in turn determines whether light is passing through the pixel.

[0059] The LCD **200** further includes liquid crystals **217** disposed between the panels **201** and **203** and particularly disposed in relation to the pixel region approximately defined by the transparent electrode **206** of the TFT-array panel **201**. Spacers **219** are placed between the panels **201** and **203** at regular intervals to maintain the cell gaps and the space between the panels. Generally, these spacers **219** are sprayed onto the color filter panel **203**. Moreover, the panels **201** and **203** are seal together via a seal **225**, which can be cured with heat and pressure. The LCD further includes a short **223** contacting the TFT-array panel **201** and the color filter panel **203**. It will be noted, that upon complete assembly of the LCD, typically the final step is to fill the voids between the panels **201** and **203** with liquid crystal material.

[0060] Referring to FIG. **3** a cross-sectional view of a portion of a monolithic article used for processing LCD articles, such as a stage or LCD glass substrate effector is illustrated according to one embodiment. As used herein, reference to a monolithic article **300** is intended to refer to a single and integral mass of material, which is typically formed as one piece. Generally, the monolithic article **300** can be formed using processes such as casting, molding, pressing, or extruding. For example, in the case of parts having complex shapes (e.g., LCD glass substrate effectors), or hollow components (e.g., tubes), slip casting may be used. While, components having less complex contours or solid structures (e.g., a LCD stage), may be formed by molding.

[0061] According to one embodiment, the monolithic article **300** includes a body portion **301** and a surface portion **303**. Generally, the surface portion **303** includes at least a portion of the upper surface **305** but is not limited to the upper surface **305** and can extend a distance into the body portion **301**, as illustrated in FIG. **3**.

[0062] Notably, the monolithic article **300** includes an electrostatic dissipative material. As used herein, an electrostatic dissipative material includes a material that has a volume resistivity (R_v) within a range between about 1.0×10^5 Ωcm and about 1.0×10^9 Ωcm. In one embodiment, the volume